ADC0820
8-Bit High Speed µP Compatible A/D Converter with Track/Hold Function

General Description
By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 µs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/µs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications
- Resolution: 8 Bits
- Conversion Time: 2.5 µs Max (RD Mode)
- Low Power: 75 mW Max
- Total Unadjusted Error: ± 1/2 LSB and ± 1 LSB

Features
- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply — 5 VCC
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than VCC
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package
- 20-pin shrink small outline package (SSOP)

Connection and Functional Diagrams

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### Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Total Unadjusted Error</th>
<th>Package</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC0820BCV</td>
<td>±½ LSB</td>
<td>V20A — Molded Chip Carrier</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>ADC0820BCWM</td>
<td>±½ LSB</td>
<td>M20B — Wide Body Small Outline</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>ADC0820BCN</td>
<td>±½ LSB</td>
<td>N20A — Molded DIP</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>ADC0820CCJ</td>
<td>±1 LSB</td>
<td>J20A — Cerrip</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>ADC0820CCWM</td>
<td>±1 LSB</td>
<td>M20B — Wide Body Small Outline</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>ADC0820CIWM</td>
<td>±1 LSB</td>
<td>M20B — Wide Body Small Outline</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>ADC0820CCN</td>
<td>±1 LSB</td>
<td>N20A — Molded DIP</td>
<td>0°C to +70°C</td>
</tr>
</tbody>
</table>

![Connection and Functional Diagrams](image)
### Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{CC}$) 10V
Logic Control Inputs $-0.2V$ to $V_{CC} +0.2V$
Voltage at Other Inputs and Output $-0.2V$ to $V_{CC} +0.2V$
Storage Temperature Range $-65˚C$ to $+150˚C$
Package Dissipation at $T_A = 25˚C$ 875 mW
Input Current at Any Pin (Note 5) 1 mA
Package Input Current (Note 5) 4 mA
ESD Susceptability (Note 9) 1200V
Lead Temp. (Soldering, 10 sec.) 260˚C

### Supply Voltage

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual-In-Line Package (plastic)</td>
<td>260˚C</td>
</tr>
<tr>
<td>Dual-In-Line Package (ceramic)</td>
<td>300˚C</td>
</tr>
<tr>
<td>Surface Mount Package</td>
<td>215˚C</td>
</tr>
<tr>
<td>Vapor Phase (60 sec.)</td>
<td>220˚C</td>
</tr>
<tr>
<td>Infrared (15 sec.)</td>
<td>-</td>
</tr>
</tbody>
</table>

### Operating Ratings (Notes 1, 2)

Temperature Range $T_{MIN} < T_A < T_{MAX}$
ADC0820CCJ $-40˚C < T_A < 85˚C$
ADC0820CIWM $-40˚C < T_A < 85˚C$
ADC0820BCN, ADC0820CCN $0˚C < T_A < 70˚C$
ADC0820BCV $0˚C < T_A < 70˚C$
ADC0820BCWM, ADC0820CCWM $0˚C < T_A < 70˚C$

### Converter Characteristics

The following specifications apply for RD mode (pin 7=0), $V_{CC}$=5V, $V_{REF(+)}$=5V and $V_{REF(-)}$=GND unless otherwise specified. Boldface limits apply from $T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_j = 25˚C$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>ADC0820BCN, ADC0820CCN</th>
<th>ADC0820BCV, ADC0820BCWM</th>
<th>ADC0820CCWM, ADC0820CIWM</th>
<th>Limit Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>Typ</td>
<td>Tested Limit (Note 6)</td>
<td>Design Limit (Note 7)</td>
<td>Typ</td>
<td>Tested Limit (Note 6)</td>
</tr>
<tr>
<td>ADC0820CCJ</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>ADC0820BCN, BCWM</td>
<td>2.3</td>
<td>1.00</td>
<td>2.3</td>
<td>1.2</td>
<td>kΩ</td>
</tr>
<tr>
<td>ADC0820CCJ</td>
<td>±1</td>
<td>±1/2</td>
<td>±1/2</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>ADC0820CCN, CCWM, CIWM, ADC0820CCMSA</td>
<td>2.3</td>
<td>6</td>
<td>2.3</td>
<td>5.3</td>
<td>6</td>
</tr>
<tr>
<td>Minimum Reference Resistance</td>
<td>2.3</td>
<td>1.00</td>
<td>2.3</td>
<td>1.2</td>
<td>kΩ</td>
</tr>
<tr>
<td>Maximum Reference Resistance</td>
<td>±1</td>
<td>±1/2</td>
<td>±1/2</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>Maximum $V_{REF(+)}$ Input Voltage</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Minimum $V_{REF(-)}$ Input Voltage</td>
<td>$V_{REF(-)}$</td>
<td>$V_{REF(-)}$</td>
<td>$V_{REF(-)}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Maximum $V_{REF(-)}$ Input Voltage</td>
<td>$V_{REF(-)}$</td>
<td>$V_{REF(-)}$</td>
<td>$V_{REF(-)}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Maximum $V_IN$ Input Voltage</td>
<td>$V_{CC}+0.1$</td>
<td>$V_{CC}+0.1$</td>
<td>$V_{CC}+0.1$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Minimum $V_{REF}$ Input Voltage</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Maximum Analog Sensitivity</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>$V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>±1/16</td>
<td>±1/16</td>
<td>±1/16</td>
<td>±1/16</td>
<td>±1/16</td>
</tr>
</tbody>
</table>
## DC Electrical Characteristics

The following specifications apply for \( V_{CC} = 5\text{V} \), unless otherwise specified. **Boldface limits apply from \( T_{\text{MIN}} \) to \( T_{\text{MAX}} \); all other limits \( T_A = T_J = 25^\circ\text{C} \).

<table>
<thead>
<tr>
<th>Parameter Conditions</th>
<th>ADC0820BCN, ADC0820CCN ADC0820CCWM, ADC0820BCWM</th>
<th>Limit Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Type (Note 6) Tested Limit (Note 7) Design Limit (Note 8)</td>
<td></td>
</tr>
</tbody>
</table>

### Input Voltage

- **V(IN, Logical “1”])**  
  \( V_{CC}=5.25\text{V} \) \( CS, WR, RD \)  
  - Mode  
  - Limit: 2.0  
  - Design Limit: 2.0  
  - Units: \( \text{V} \)

- **V(IN, Logical “0”])**  
  \( V_{IN}=4.75\text{V} \) \( CS, WR, RD \)  
  - Mode  
  - Limit: 0.8  
  - Design Limit: 0.8  
  - Units: \( \text{V} \)

### Input Current

- **I(IN, Logical “1”)**  
  \( V_{IN}=5\text{V} \) \( CS, RD \)  
  - Limit: 0.005  
  - Units: \( \mu\text{A} \)

- **I(IN, Logical “0”)**  
  \( V_{IN}=0\text{V} \) \( CS, RD, WR \)  
  - Limit: −0.005  
  - Units: \( \mu\text{A} \)

### Output Voltage

- **V(OUT, Logical “1”)**  
  \( V_{CC}=4.75\text{V} \), \( I_{OUT}=-360\mu\text{A} \); \( DB0-DB7, \text{OFL, INT} \)  
  - Limit: 2.4  
  - Units: \( \text{V} \)

- **V(OUT, Logical “0”)**  
  \( DB0-DB7, \text{OFL, INT} \)  
  - Limit: 0.4  
  - Units: \( \text{V} \)

### Output Current

- **I(SOURCE), Output INT**  
  \( V_{OUT}=5\text{V} \); \( DB0-DB7, \text{OFL, INT, RDY} \)  
  - Limit: −12  
  - Units: \( \text{mA} \)

- **I(SINK), Output Sink INT**  
  \( V_{OUT}=5\text{V} \); \( DB0-DB7, \text{OFL, INT, RDY} \)  
  - Limit: 14  
  - Units: \( \text{mA} \)

### Supply Current

- **I(CC), Supply Current**  
  \( CS=WR=RD=0 \)  
  - Limit: 7.5  
  - Units: \( \text{mA} \)

## AC Electrical Characteristics

The following specifications apply for \( V_{CC}=5\text{V}, t_{\text{r}}=t_{\text{f}}=20\text{ ns}, V_{\text{REF}(+)}=5\text{V}, V_{\text{REF}(-)}=0\text{V} \) and \( T_A=25^\circ\text{C} \) unless otherwise specified.

| Parameter Conditions | Type (Note 6) Tested Limit (Note 7) Design Limit (Note 8) Units |
|----------------------|---------------------------------------------------------------|-------------|

### Conversion Time

- **t(CRD), Conversion Time for RD Mode**  
  Pin 7 = 0, Figure 2  
  - Limit: 1.6  
  - Units: \( \mu\text{s} \)

- **t(ACC0), Access Time (Delay from Pin 7 = 0, Figure 2 to Output Valid)**  
  Pin 7 = 0, Figure 2  
  - Limit: \( t_{\text{CRD}} \times 20 \)  
  - Units: \( \text{ns} \)

- **t(WR-RD), Conversion Time for Pin 7 = V CC; t WR = 600 ns, t RD = 600 ns; Figures 3, 4**  
  - Limit: 1.52  
  - Units: \( \mu\text{s} \)

- **I(WR), Write Time**  
  Min Pin 7 = \( V_{CC} \); Figures 3, 4  
  - Limit: 600  
  - Units: \( \text{ns} \)

- **I(WR), Write Time**  
  Max (Note 4) See Graph  
  - Limit: 50  
  - Units: \( \mu\text{s} \)

- **I(ACC1), Access Time (Delay from Pin 7 = V CC, t RD < t I; Figure 3 to Output Valid)**  
  Pin 7 = \( V_{CC} \); \( t_{\text{RD}} \times 1 \); Figure 3  
  - Limit: 190  
  - Units: \( \text{ns} \)

- **I(ACC1) = 15\text{pF}, Figure 3**  
  - Limit: 210  
  - Units: \( \text{ns} \)

- **I(ACC1) = 100\text{pF}, Figure 3**  
  - Limit: 320  
  - Units: \( \text{ns} \)
The following specifications apply for $V_{CC}=5V$, $t_{r}=20\,\text{ns}$, $V_{\text{REF}(+)}=5V$, $V_{\text{REF}(-)}=0V$ and $T_{A}=25^\circ\text{C}$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (Note 6)</th>
<th>Tested Limit (Note 7)</th>
<th>Design Limit (Note 8)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{ACC2}}$, Access Time (Delay from Falling Edge of RD to Output Valid)</td>
<td>Pin 7 = $V_{CC}$, $t_{\text{RD}}&gt;t_{I}$; Figure 4 $C_{L}=15,\text{pF}$</td>
<td>70</td>
<td>120</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_{L}=100,\text{pF}$</td>
<td>90</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{ACC3}}$, Access Time (Delay from Rising Edge of RDY to Output Valid)</td>
<td>$R_{\text{PULLUP}} = 1k$ and $C_{L} = 15,\text{pF}$</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{I}$, Internal Comparison Time</td>
<td>Pin 7=$V_{CC}$; Figures 4, 5 $C_{L}=50,\text{pF}$</td>
<td>800</td>
<td>1300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{IH}}, t_{\text{IL}}$, TRI-STATE Control (Delay from Rising Edge of RD to Hi-Z State)</td>
<td>$R_{L}=1k$, $C_{L}=10,\text{pF}$</td>
<td>100</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{WR}}$, Delay from Rising Edge of WR to Falling Edge of INT</td>
<td>Pin 7 = $V_{CC}$, $C_{L}=50,\text{pF}$ $t_{\text{WR}}&gt;t_{I}$; Figure 4 $t_{\text{WR}}&lt;t_{I}$; Figure 3</td>
<td>$t_{\text{WR}}+200$</td>
<td>$t_{I}$</td>
<td>$t_{\text{WR}}+290$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{\text{RDY}}$, Delay from Rising Edge of RDY to Rising Edge of INT</td>
<td>Figures 2, 3, 4</td>
<td>125</td>
<td>225</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{WR}}, t_{\text{RD}}$, Delay from Rising Edge of WR to Rising Edge of INT</td>
<td>Figure 5, $C_{L}=50,\text{pF}$</td>
<td>175</td>
<td>270</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{RD}}$, Delay from CS to RDY</td>
<td>Figure 2, $C_{L}=50,\text{pF}$, Pin 7 =0</td>
<td>50</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{ID}}$, Delay from INT to Output Valid</td>
<td>Figure 5</td>
<td>20</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{ID}}$, Delay from RD to INT</td>
<td>Pin 7=$V_{CC}$, $t_{\text{RD}}&lt;t_{I}$ Figure 3</td>
<td>200</td>
<td>290</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{IN}}$, Delay from End of Conversion to Next Conversion</td>
<td>Figures 2, 3, 4, 5 (Note 4) See Graph</td>
<td>500</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Slew Rate, Tracking</td>
<td>0.1</td>
<td></td>
<td></td>
<td></td>
<td>$V/\mu\text{s}$</td>
</tr>
<tr>
<td>$C_{\text{VIN}}$, Analog Input Capacitance</td>
<td>45</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{\text{OUT}}$, Logic Output Capacitance</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{\text{IN}}$, Logic Input Capacitance</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if $t_{\text{WR}}$ or $t_{\text{RD}}$ is shorter than the minimum value specified. See Accuracy vs $t_{\text{WR}}$ and Accuracy vs $t_{\text{RD}}$ graphs.

Note 5: When the input voltage ($V_{\text{IN}}$) at any pin exceeds the power supply rails ($V_{\text{IN}}<V_{-}$ or $V_{\text{IN}}>V_{+}$) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

Note 6: Totals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: Human body model, 100 pF discharged through a 1.5 kΩ resistor.
TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Note: On power-up the state of INT can be high or low.

FIGURE 2. RD Mode (Pin 7 is Low)
Timing Diagrams (Continued)

FIGURE 3. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)

FIGURE 4. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

FIGURE 5. WR-RD Mode (Pin 7 is High)
Stand-Alone Operation
Typical Performance Characteristics

Logic Input Threshold Voltage vs Supply Voltage

Conversion Time (RD Mode) vs Temperature

Power Supply Current vs Temperature (not including reference ladder)

Accuracy vs \( t_{WR} \)

Accuracy vs \( t_{HD} \)

Accuracy vs \( t_p \)

Accuracy vs \( V_{REF} \)  
\( V_{REF} = V_{REF(+)} - V_{REF(-)} \)

\( t_{I} \), Internal Time Delay vs Temperature

Output Current vs Temperature

\( ^*1 \text{ LSB} = \frac{V_{REF}}{256} \)
<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V \text{IN}</td>
<td>Analog input; range = \text{GND} \leq V \text{IN} \leq V \text{CC}</td>
</tr>
<tr>
<td>2</td>
<td>DB0</td>
<td>TRI-STATE data output — bit 0 (LSB)</td>
</tr>
<tr>
<td>3</td>
<td>DB1</td>
<td>TRI-STATE data output — bit 1</td>
</tr>
<tr>
<td>4</td>
<td>DB2</td>
<td>TRI-STATE data output — bit 2</td>
</tr>
<tr>
<td>5</td>
<td>DB3</td>
<td>TRI-STATE data output — bit 3</td>
</tr>
<tr>
<td>6</td>
<td>WR</td>
<td>WR-RD Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>/RDY</td>
</tr>
<tr>
<td>7</td>
<td>Mode</td>
<td>Mode selection input — it is internally tied to GND through a 50 µA current source.</td>
</tr>
<tr>
<td>8</td>
<td>RD</td>
<td>WR-RD Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RD Mode: When mode is low</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RD-RD Mode: When mode is high</td>
</tr>
<tr>
<td>9</td>
<td>INT</td>
<td>WR-RD Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>INT going low indicates that the conversion is completed and the data result is in the output latch. INT will go low, \approx 800 ns (the preset internal time out, t_I) after the rising edge of WR (see Figure 4); or INT will go low after the falling edge of RD, if RD goes low prior to the 800 ns time out (see Figure 3). INT is reset by the rising edge of RD or CS (see Figures 3, 4).</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>11</td>
<td>V_{\text{REF}(-)}</td>
<td>The bottom of resistor ladder, voltage range: \text{GND} \leq V_{\text{REF}(-)} \leq V_{\text{REF}(+)} (Note 5)</td>
</tr>
<tr>
<td>12</td>
<td>V_{\text{REF}(+)}</td>
<td>The top of resistor ladder, voltage range: \text{V}<em>{\text{REF}(-)} \leq V</em>{\text{REF}(+)} \leq V_{\text{CC}} (Note 5)</td>
</tr>
<tr>
<td>13</td>
<td>CS</td>
<td>CS must be low in order for the RD or WR to be recognized by the converter.</td>
</tr>
<tr>
<td>14</td>
<td>DB4</td>
<td>TRI-STATE data output — bit 4</td>
</tr>
<tr>
<td>15</td>
<td>DB5</td>
<td>TRI-STATE data output — bit 5</td>
</tr>
<tr>
<td>16</td>
<td>DB6</td>
<td>TRI-STATE data output — bit 6</td>
</tr>
<tr>
<td>17</td>
<td>DB7</td>
<td>TRI-STATE data output — bit 7 (MSB)</td>
</tr>
<tr>
<td>18</td>
<td>OFL</td>
<td>Overflow output if the analog input is higher than the \text{V}_{\text{REF}(+)}; OFL will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit). This output is always active and does not go into TRI-STATE as DB0–DB7 do.</td>
</tr>
<tr>
<td>19</td>
<td>NC</td>
<td>No connection</td>
</tr>
<tr>
<td>20</td>
<td>V_{\text{CC}}</td>
<td>Power supply voltage</td>
</tr>
</tbody>
</table>

### 1.0 Functional Description

#### 1.1 GENERAL OPERATION

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (Figure 1). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word. The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor
1.0 Functional Description (Continued)

ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the “sampled-data” comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

1.2 THE SAMPLED-DATA COMPARATOR

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively coupled input (Figures 6, 7). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter’s input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter’s feedback switch (Figure 6) are closed. In this interval, C is charged to the connected input (V1) less the inverter’s bias voltage (VB, approximately 1.2V). In the second cycle (Figure 7), these two switches are opened and the other (V2) input’s switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter’s open loop gain. The inverter’s input (VBS) becomes

\[ V_{BS} = \frac{V1 - V2}{C + C_S} \]

and the output will go high or low depending on the sign of \( V_{BS} - V_B \).

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 8), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter’s input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

1.3 ARCHITECTURE

In the ADC0820, one bank of 15 comparators is used in each 4-bit flash A/D converter (Figure 12). The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.

When a typical conversion is started, the WR line is brought low. At this instant the MS comparators go from zeroing to comparison mode (Figure 11). When WR is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the RD line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When RD goes low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 11 also outlines how the converter’s interface timing relates to its analog input (VA0). In WR-RD mode, VA0 is mea-
1.0 Functional Description (Continued)

sured while WR is low. In RD mode, sampling occurs during the first 800 ns of RD. Because of the input connections to the ADC0820’s LS and MS comparators, the converter has the ability to sample \( V_{IN} \) at one instant (Section 2.4), despite the fact that two separate 4-bit conversions are being done. More specifically, when WR is low the MS flash is in compare mode (connected to \( V_{IN} \)), and the LS flash is in zero mode (also connected to \( V_{IN} \)). Therefore both flash ADCs sample \( V_{IN} \) at the same time.

1.4 DIGITAL INTERFACE

The ADC0820 has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling RD low until output data appears. An INT line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

When in RD mode, the comparator phases are internally triggered. At the falling edge of RD, the MS flash converter goes from zero to compare mode and the LS ADC’s comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the WR input; however, there are two options for reading the output data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for INT to go low before reading the conversion result (Figure 10). INT will typically go low 800 ns after WR’s rising edge. However, if a shorter conversion time is desired, the processor need not wait for INT and can exercise a read after only 600 ns (Figure 9). If this is done, INT will immediately go low and data will appear at the outputs.

![FIGURE 9. WR-RD Mode (Pin 7 is High and t_{RD} < t_{INT})](image)

![FIGURE 10. WR-RD Mode (Pin 7 is High and t_{RD} > t_{INT})](image)

Stand-Alone

For stand-alone operation in WR-RD mode, CS and RD can be tied low and a conversion can be started with WR. Data will be valid approximately 800 ns following WR’s rising edge.

WR-RD Mode (Pin 7 is High) Stand-Alone Operation

![FIGURE 9. WR-RD Mode (Pin 7 is High and t_{RD} < t_{INT})](image)

![FIGURE 10. WR-RD Mode (Pin 7 is High and t_{RD} > t_{INT})](image)
OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, WR has a maximum width spec of 50 µs. When the MS flash ADC’s sampled-data comparators (Section 1.2) are in comparison mode (WR is low), the input capacitors (C, Figure 8) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (Section 1.3), a new conversion cannot be started until this phase is complete. The minimum spec for this time ($t_z$, Figures 2, 3, 4, 5) is 500 ns.

**FIGURE 11. Operating Sequence (WR-RD Mode)**

Note: MS means most significant
LS means least significant
2.0 Analog Considerations

2.1 REFERENCE AND INPUT

The two $V_{\text{REF}}$ inputs of the ADC0820 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{\text{IN}}(\text{+})$ and $V_{\text{IN}}(\text{-})$. By reducing $V_{\text{REF}} = V_{\text{REF}(\text{+})} - V_{\text{REF}(\text{-})}$ to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{\text{REF}} = 2V$ then 1 LSB = 7.8 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the $V_{\text{REF}}$ source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{\text{REF}}(\text{-})$ sets the input level which produces a digital output of all zeroes. Though $V_{\text{IN}}$ is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. Figure 13 shows some of the configurations that are possible.

2.2 INPUT CURRENT

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D’s sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

[$\text{Figure 14}$. When a conversion starts (WR low, WR-RD mode), all input switches close, connecting $V_{\text{IN}}$ to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, $V_{\text{IN}}$ still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (Section 1.3). In other words, the LS ADC uses $V_{\text{IN}}$ as its zero-phase input.

The input capacitors must charge to the input voltage through the voltage resistor of the analog switches (about 5 kΩ to 10 kΩ). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in Figure 15. As $R_S$ increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that WR is low. Since other factors force this time to be at least 600 ns, input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow $R_S$ to be 1.5 kΩ without lengthening WR to give $V_{\text{IN}}$ more time to settle.

**FIGURE 13. Analog Input Options**
2.0 Analog Considerations (Continued)

2.3 INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_IN, will not degrade the A/D's performance in most cases. In effect the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while WR is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_IN terminal.

2.4 INHERENT SAMPLE-HOLD

Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least 1/2 LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5 µs, the time through which V_IN must be 1/2 LSB stable is much smaller. Since the MS flash ADC uses V_IN as its "compare" input and the LS ADC uses V_IN as its "zero" input, the ADC0820 only "samples" V_IN when WR is low (Sections 1.3 and 2.2). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_IN approximately 100 ns after the rising edge of WR (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/µs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 µs would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7 kHz waveforms.
3.0 Typical Applications

8-Bit Resolution Configuration

9-Bit Resolution Configuration
3.0 Typical Applications (Continued)

- V_IN=3 kHz max ± 4Vp
- No track-and-hold needed
- Low power consumption

### Telecom A/D Converter

- DS005501-28

### Multiple Input Channels

- DS005501-29

### 8-Bit 2-Quadrant Analog Multiplier

- DS005501-30

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3.0 Typical Applications (Continued)

Fast Infinite Sample-and-Hold

[Diagram of a circuit with labels and components]

DS06500-31
3.0 Typical Applications

Digital Waveform Recorder

- 1.3M samples/sec
- 4x memory
Physical Dimensions inches (millimeters) unless otherwise noted

Hermetic Dual-In-Line Package (J)
Order Number ADC0820CCJ
NS Package Number J20A
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