MM54HC166/MM74HC166 8-Bit Parallel In/Serial Out Shift Registers

General Description
The MM54HC166/MM74HC166 high speed 8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These Parallel-In or Serial-In, Serial-Out shift registers feature gated CLOCK inputs and an overriding CLEAR input. The load mode is established by the SHIFT/LOAD input. When high, this input enables the SERIAL INPUT and couples the eight flip-flops for serial shifting with each clock pulse. When low, the PARALLEL INPUTS are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the CLOCK pulse through a 2-input NOR gate, permitting one input to be used as a clock enable or CLOCK INHIBIT function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The CLOCK INHIBIT input should be changed to the high level only while the clock input is high. A direct CLEAR input overrides all other inputs, including the CLOCK, and sets all flip-flops to zero.

The 54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to VCC and Ground.

Features
- Typical propagation delay:
- Wide operating supply voltage range: 2V–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Function Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Clear</th>
<th>Shift/Load</th>
<th>Clock Inhibit</th>
<th>Clock</th>
<th>Serial</th>
<th>Parallel (A...H)</th>
<th>Outputs (Q0, Q10)</th>
<th>Internal Outputs (Q0, Q10)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>Q0</td>
<td>Q0</td>
<td>QH0</td>
<td>QH1</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>↑</td>
<td>X</td>
<td>a...h</td>
<td>a</td>
<td>h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>↑</td>
<td>H</td>
<td>X</td>
<td>Q0</td>
<td>Q0</td>
<td>QH0</td>
<td>QH1</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>H</td>
<td>↑</td>
<td>X</td>
<td>Q0</td>
<td>Q0</td>
<td>QH0</td>
<td>QH1</td>
</tr>
</tbody>
</table>

H = High Level (steady state), L = Low Level (steady state)
X = Don’t Care (any input, including transitions)
↑ = Transition from low to high level
a...h = The level of steady-state input at inputs A through H, respectively
Q0, Q10, Q0, Q10 = The level of Q0, Q10, respectively, before the indicated steady-state input conditions were established
Q0, Q10 = The level of Q0, Q10, respectively, before the most recent ↑ transition of the clock
### Absolute Maximum Ratings (Notes 1 & 2)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- **Supply Voltage (V\(_{CC}\))**
  - Min: -0.5V, Max: +7.0V

- **DC Input Voltage (V\(_{IN}\))**
  - Min: -1.5V to V\(_{CC}\), Max: +1.5V

- **DC Output Voltage (V\(_{OUT}\))**
  - Min: -0.5V to V\(_{CC}\), Max: +0.5V

- **Clamp Diode Current (I\(_{IK}, I_{OK}\))**
  - Max: 20 mA

- **DC Output Current, per Pin (I\(_{OUT}\))**
  - Max: 25 mA

- **DC V\(_{CC}\) or GND Current, per Pin (I\(_{CC}\))**
  - Max: 50 mA

- **Storage Temperature Range (T\(_{STG}\))**
  - Min: -65°C, Max: +150°C

- **Power Dissipation (P\(_D\))**
  - Min: 600 mW, S.O. Package only: 500 mW

#### Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V(_{CC}))</td>
<td></td>
<td>2</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>DC Input or Output Voltage (V(<em>{IN}, V</em>{OUT}))</td>
<td></td>
<td>0</td>
<td>V(_{CC})</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temp. Range (T(_A))</td>
<td>MM74HC</td>
<td>-40</td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>MM54HC</td>
<td>-55</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Input Rise or Fall Times (t(<em>r, t</em>{f}))</td>
<td></td>
<td>1000 ns</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>V(_{CC}) = 2.0V</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>V(_{CC}) = 4.5V</td>
<td>500 ns</td>
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<tr>
<td></td>
<td>V(_{CC}) = 6.0V</td>
<td>400 ns</td>
<td></td>
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</table>

#### DC Electrical Characteristics (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>V(_{CC})</th>
<th>T(_A) = -25°C</th>
<th>T(_A) = -40°C to +85°C</th>
<th>T(_A) = -55°C to +125°C</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{IH})</td>
<td>Minimum High</td>
<td></td>
<td>2.0V</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>V(_{IL})</td>
<td>Maximum Low</td>
<td></td>
<td>2.0V</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Level Input</td>
<td></td>
<td>4.5V</td>
<td>1.35</td>
<td>1.35</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Voltage**</td>
<td></td>
<td>6.0V</td>
<td>1.8</td>
<td>1.8</td>
<td>1.8</td>
<td>V</td>
</tr>
<tr>
<td>V(_{OH})</td>
<td>Minimum High</td>
<td></td>
<td>V(<em>{IN}) - V(</em>{IH}) or V(_{IL})</td>
<td>2.0V</td>
<td>2.0</td>
<td>1.9</td>
<td>V</td>
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<tr>
<td></td>
<td>Level Output Voltage</td>
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<td>4.5V</td>
<td>4.5</td>
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<td>6.0V</td>
<td>6.0</td>
<td>5.9</td>
<td>5.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V(<em>{IN}) - V(</em>{IH}) or V(_{IL})</td>
<td>4.5V</td>
<td>4.2</td>
<td>3.98</td>
<td>V</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>6.0V</td>
<td>5.7</td>
<td>5.48</td>
<td>V</td>
</tr>
<tr>
<td>V(_{OL})</td>
<td>Minimum Low</td>
<td></td>
<td>V(<em>{IN}) - V(</em>{IH}) or V(_{IL})</td>
<td>2.0V</td>
<td>0</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Level Output Voltage</td>
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<td></td>
<td>4.5V</td>
<td>0</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6.0V</td>
<td>0</td>
<td>0.1</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>V(<em>{IN}) - V(</em>{IH}) or V(_{IL})</td>
<td>4.5V</td>
<td>0.2</td>
<td>0.26</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6.0V</td>
<td>0.2</td>
<td>0.26</td>
<td>V</td>
</tr>
<tr>
<td>I(_{IN})</td>
<td>Maximum Input Current</td>
<td></td>
<td></td>
<td>V(<em>{IN}) - V(</em>{CC}) or GND</td>
<td>6.0V</td>
<td>±0.1</td>
<td>±1.0</td>
</tr>
<tr>
<td>I(_{CC})</td>
<td>Maximum Quiescent Supply Current</td>
<td></td>
<td></td>
<td>V(<em>{IN}) - V(</em>{CC}) or GND</td>
<td>6.0V</td>
<td>8.0</td>
<td>80</td>
</tr>
</tbody>
</table>

**Notes:**
1. Absolute Maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified at all voltages are referenced to ground.
3. Power dissipation temperature derating—plastic “N” package: -12 mW/°C from 65°C to 85°C; ceramic “J” package: -12 mW/°C from 100°C to 125°C.
4. For a power supply of 5V ±10%, the worst-case output voltages (V\(_{OH}\) and V\(_{OL}\)) occur for HC at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst-case V\(_{IH}\) and V\(_{IL}\) occur at V\(_{CC}\) = 5.5V and 4.5V, respectively. (The V\(_{IH}\) value at 5.5V is 3.85V.) The worst-case leakage current (I\(_{IH}, I_{IC}, I_{LZ}\)) occur for CMOS at the higher voltage and so the 6.0V values should be used.
5. **V\(_{IL}\) limits are currently tested at 20% of V\(_{CC}\). The above V\(_{IL}\) specification (30% of V\(_{CC}\)) will be implemented no later than Q1, CY’89.
### AC Electrical Characteristics

**C_{L} = 50 \text{ pF}, \tau_{r} - \tau_{f} = 6 \text{ ns unless otherwise noted}**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>( V_{CC} )</th>
<th>( T_{A} = -25^\circ C )</th>
<th>( T_{A} = -40^\circ C ) to +85(^\circ C )</th>
<th>( T_{A} = -55^\circ C ) to +125(^\circ C )</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{MAX} )</td>
<td>Maximum Operating Frequency</td>
<td>2.0V</td>
<td>31</td>
<td>5</td>
<td>4.2</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>25</td>
<td>21</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>29</td>
<td>25</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( t_{PHL}/t_{PLH} )</td>
<td>Maximum Propagation Delay Clock to ( Q_H )</td>
<td>2.0V</td>
<td>14</td>
<td>175</td>
<td>210</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>28</td>
<td>35</td>
<td>42</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>24</td>
<td>30</td>
<td>36</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{PHL}/t_{PLH} )</td>
<td>Maximum Propagation Delay Clear to ( Q_H )</td>
<td>2.0V</td>
<td>11</td>
<td>165</td>
<td>195</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>26</td>
<td>35</td>
<td>39</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>22</td>
<td>30</td>
<td>33</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SU} )</td>
<td>Minimum Setup Time Shift/Load to Clock</td>
<td>2.0V</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>16</td>
<td>20</td>
<td>24</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>14</td>
<td>18</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SU} )</td>
<td>Minimum Setup Time Data before Clock</td>
<td>2.0V</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>16</td>
<td>20</td>
<td>24</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>14</td>
<td>18</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{REM} )</td>
<td>Minimum Removal Time Clear to Clock</td>
<td>2.0V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{H} )</td>
<td>Maximum Hold Time Data after Clock</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
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<tr>
<td>( t_{R} )</td>
<td>Maximum Output Rise and Fall Time</td>
<td>2.0V</td>
<td>7</td>
<td>75</td>
<td>110</td>
<td>ns</td>
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<td></td>
<td></td>
<td>4.5V</td>
<td>15</td>
<td>95</td>
<td>110</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>13</td>
<td>19</td>
<td>22</td>
<td>ns</td>
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<tr>
<td>( t_{W} )</td>
<td>Minimum Pulse Width Clock or Clear</td>
<td>2.0V</td>
<td>80</td>
<td>100</td>
<td>120</td>
<td>ns</td>
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<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>16</td>
<td>20</td>
<td>24</td>
<td>ns</td>
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<td></td>
<td></td>
<td>6.0V</td>
<td>14</td>
<td>16</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>C_{pd}</td>
<td>Power Dissipation Capacitance (Note 5) (per package)</td>
<td>100</td>
<td>pF</td>
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<td>C_{in}</td>
<td>Maximum Input Capacitance</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**Note:** C_{pd} determines the no load dynamic power consumption, P_{D} = C_{PD} \cdot V_{CC} \cdot f / + I_{CC}, and the no load dynamic current consumption, I_{S} = C_{PD} \cdot V_{CC} / + V_{CC}.
Logic Diagram

Typical Clear, Shift, Load, Inhibit and Shift Sequences
MM54HC166/MM74HC166 8-Bit Parallel In/Serial Out Shift Registers

Physical Dimensions inches (millimeters)

Order Number MM54HC166 or MM74HC166
NS Package Number M16A

Order Number MM54HC166 or MM74HC166
NS Package Number N16E

LIFE SUPPORT POLICY

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