MM74HC00 Quad 2-Input NAND Gate

General Description
These NAND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to VCC and ground.

Features
- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 µA maximum (74HC Series)
- Low input current: 1 µA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagram

[Diagram showing the connection and logic diagram of the MM74HC00 quad 2-input NAND gate.]
### Absolute Maximum Ratings (Notes 2, 1)

- **Supply Voltage** ($V_{CC}$): −0.5 to +7.0V
- **DC Input Voltage** ($V_{IN}$): −1.5 to $V_{CC}$ +1.5V
- **DC Output Voltage** ($V_{OUT}$): −0.5 to $V_{CC}$ +0.5V
- **Clamp Diode Current** ($I_{IK}, I_{OK}$): ±20 mA
- **DC Output Current, per pin** ($I_{OUT}$): ±25 mA
- **DC $V_{CC}$ or GND Current, per pin** ($I_{CC}$): ±50 mA
- **Storage Temperature Range** ($T_{STG}$): −65˚C to +150˚C
- **Power Dissipation** ($P_D$): (Note 3) 600 mW
  - S.O. Package only: 500 mW
- **Lead Temperature** ($T_L$): (Soldering 10 seconds) 260˚C

### Operating Conditions

- **Supply Voltage** ($V_{CC}$): 2 to 6 V
- **DC Input or Output Voltage**: 0 to $V_{CC}$ V
- **Operating Temp. Range** ($T_A$): MM74HC −40 to +85˚C, MM54HC −55 to +125˚C

### DC Electrical Characteristics (Note 4)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$V_{CC}$</th>
<th>$T_A=25^\circ C$</th>
<th>74HC $T_A=-40$ to $85^\circ C$</th>
<th>54HC $T_A=-55$ to $125^\circ C$</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Minimum High Level Input Voltage</td>
<td>2.0V</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Maximum Low Level Input Voltage</td>
<td>2.0V</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Minimum High Level Output Voltage</td>
<td>$V_{IN}=V_{IH}$ or $V_{IL}$</td>
<td>2.0V</td>
<td>2.0</td>
<td>1.9</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Maximum Low Level Output Voltage</td>
<td>$V_{IN}=V_{IH}$</td>
<td>2.0V</td>
<td>0</td>
<td>0.1</td>
<td>0.1</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic “N” package: −12 mW/˚C from 65˚C to 85˚C; ceramic “J” package: −12 mW/˚C from 100˚C to 125˚C.

**Note 4:** For a power supply of 5V ± 10%, the worst case output voltages ($V_{OH}$, $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}=5.5V$ and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**Note 5:** $V_{IL}$ limits are currently tested at 20% of $V_{CC}$. The above $V_{IL}$ specification (30% of $V_{CC}$) will be implemented no later than Q1, CY’89.
## AC Electrical Characteristics

\( V_{CC} = 5V, \ T_A = 25{}^\circ C, \ C_L = 15 \ pF, \ t_r = t_f = 6 \ ns \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Guaranteed</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>15</td>
<td>ns</td>
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</tbody>
</table>

## AC Electrical Characteristics

\( V_{CC} = 2.0V \) to \( 6.0V, \ C_L = 50 \ pF, \ t_r = t_f = 6 \ ns \) (unless otherwise specified)

\( T_A = 25{}^\circ C \)

\( T_A = -40 \) to \( 85{}^\circ C \)

\( T_A = -55 \) to \( 125{}^\circ C \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>( V_{CC} )</th>
<th>( T_A = 25{}^\circ C )</th>
<th>( T_A = -40 ) to ( 85{}^\circ C )</th>
<th>( T_A = -55 ) to ( 125{}^\circ C )</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PHL} ), ( t_{PLH} )</td>
<td>Maximum Propagation Delay</td>
<td>2.0V</td>
<td>45</td>
<td>90</td>
<td>113</td>
<td>134</td>
<td>ns</td>
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<td></td>
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<td>4.5V</td>
<td>9</td>
<td>18</td>
<td>23</td>
<td>27</td>
<td>ns</td>
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<td></td>
<td></td>
<td>6.0V</td>
<td>8</td>
<td>15</td>
<td>19</td>
<td>23</td>
<td>ns</td>
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<tr>
<td>( t_{PLH} ), ( t_{PLH} )</td>
<td>Maximum Output Rise and Fall Time</td>
<td>2.0V</td>
<td>30</td>
<td>75</td>
<td>95</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5V</td>
<td>8</td>
<td>15</td>
<td>19</td>
<td>22</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.0V</td>
<td>7</td>
<td>13</td>
<td>16</td>
<td>19</td>
<td>ns</td>
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<tr>
<td>( C_{PD} )</td>
<td>Power Dissipation Capacitance (Note 6)</td>
<td>(per gate)</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Maximum Input Capacitance</td>
<td></td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
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**Note 6:** \( C_{PD} \) determines the no load dynamic power consumption, \( P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC} \), and the no load dynamic current consumption, \( I_S = C_{PD} \frac{V_{CC}^2}{f} + I_{CC} \).
Physical Dimensions

Cavity Dual-In Line Package (J)
Order Number MM54HC00J or MM74HC00J
Package J14A

Molded Dual-In Line Package (N)
Order Number MM74HC00N
Package N14A

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